Introduction to Flash Memory

Leon Romanovsky
`leon@leon.nu`

www.leon.nu

January 13, 2013

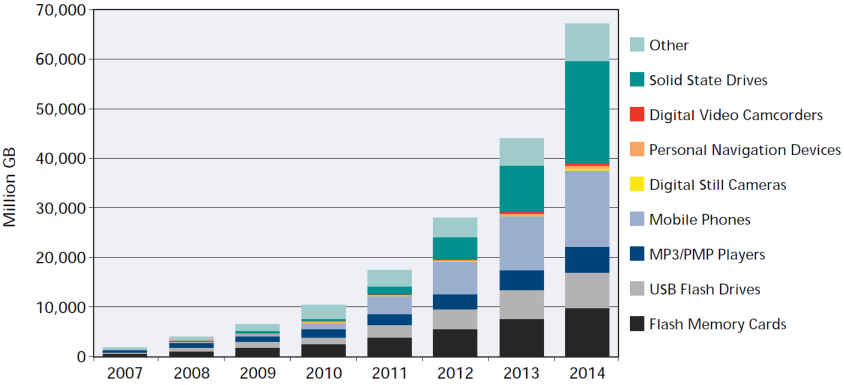
Disclaimer

Everything in this lecture shall not, under any circumstances, hold any legal liability whatsoever. Any usage of the data and information in this document shall be solely on the responsibility of the user. This lecture is not given on behalf of any company or organization.

Definition

Flash memory is a non-volatile storage device that can be electrically erased and reprogrammed.

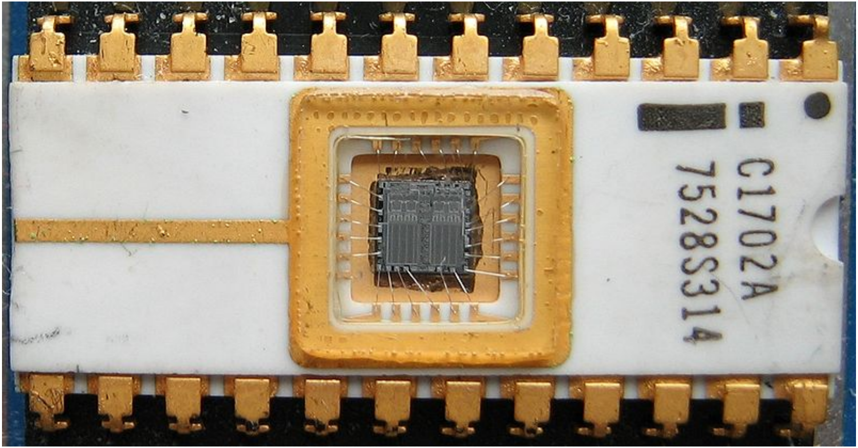
Major Markets



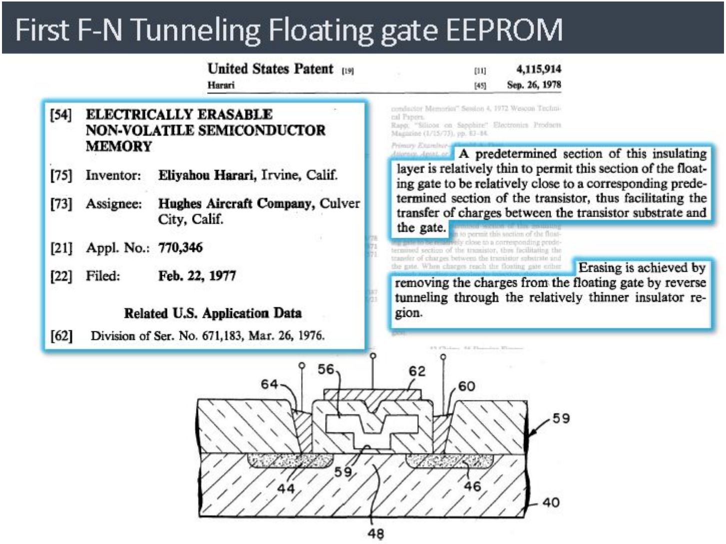
Source: Forward Insights, NAND Quarterly Insights Q3/09, www.forward-insights.com/
Report No. FI-NFL-NQI-Q309 September 2009, accessed 4/14/2010; used with permission.

Jiroft Inscription - 2600 BCE

EPROM, Dov Frohman, Intel - 1971



F-N Tunneling Floating Gate, Dr. Eli Harari - 1978



First F-N Tunneling Floating gate EEPROM

United States Patent [19] [11] **4,115,914**
Harari [45] **Sep. 26, 1978**

[54] **ELECTRICALLY ERASABLE NON-VOLATILE SEMICONDUCTOR MEMORY**

[75] Inventor: **Eliyahou Harari,** Irvine, Calif.

[73] Assignee: **Hughes Aircraft Company,** Culver City, Calif.

[21] Appl. No.: **770,346**

[22] Filed: **Feb. 22, 1977**

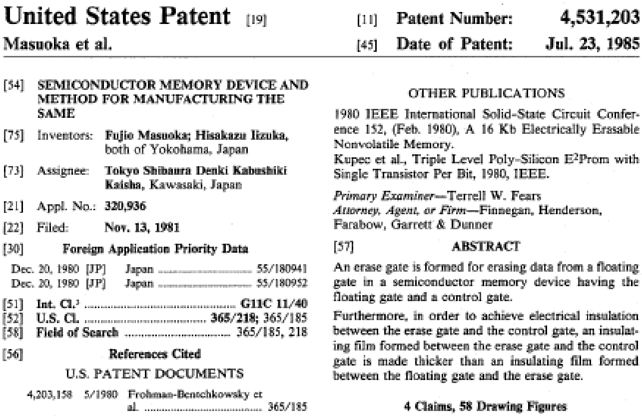
Related U.S. Application Data

[62] Division of Ser. No. 671,183, Mar. 26, 1976.

A predetermined section of this insulating layer is relatively thin to permit this section of the floating gate to be relatively close to a corresponding predetermined section of the transistor, thus facilitating the transfer of charges between the transistor substrate and the gate.

Erasing is achieved by removing the charges from the floating gate by reverse tunneling through the relatively thinner insulator region.

NOR/NAND Memory Patent, Dr. Fujio Masuoka - 1981



United States Patent [19]

Masuoka et al.

[11] **Patent Number:** **4,531,203**

[45] **Date of Patent:** **Jul. 23, 1985**

[54] **SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME**

[75] Inventors: **Fujio Masuoka; Hisakazu Iizuka,** both of Yokohama, Japan

[73] Assignee: **Tokyo Shibaura Denki Kabushiki Kaisha,** Kawasaki, Japan

[21] Appl. No.: **320,936**

[22] Filed: **Nov. 13, 1981**

[30] **Foreign Application Priority Data**

Dec. 20, 1980	[JP]	Japan	55/180941
Dec. 20, 1980	[JP]	Japan	55/180952

[51] **Int. Cl.^{3}** **G11C 11/40**
[52] **U.S. Cl.** **365/218;** 365/185
[58] **Field of Search** 365/185, 218

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,203,158 5/1980 Frohman-Bentchkowsky et al. 365/185

OTHER PUBLICATIONS

1980 IEEE International Solid-State Circuit Conference 152, (Feb. 1980), A 16 Kb Electrically Erasable Nonvolatile Memory.
Kupec et al., Triple Level Poly-Silicon E^{2}Prom with Single Transistor Per Bit, 1980, IEEE.

Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

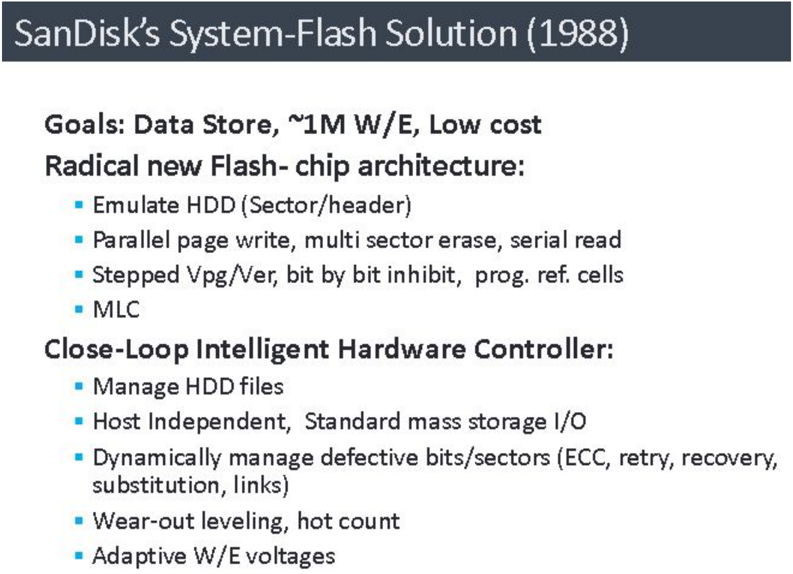
[57] **ABSTRACT**

An erase gate is formed for erasing data from a floating gate in a semiconductor memory device having the floating gate and a control gate.

Furthermore, in order to achieve electrical insulation between the erase gate and the control gate, an insulating film formed between the erase gate and the control gate is made thicker than an insulating film formed between the floating gate and the erase gate.

4 Claims, 58 Drawing Figures

Storage Flash Solution, Sandisk - 1988



SanDisk's System-Flash Solution (1988)

Goals: Data Store, ~1M W/E, Low cost

Radical new Flash- chip architecture:

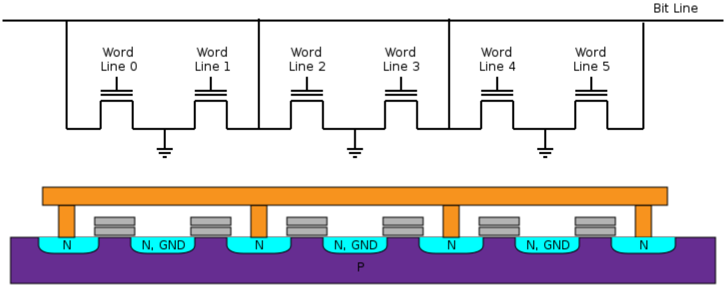
- Emulate HDD (Sector/header)
- Parallel page write, multi sector erase, serial read
- Stepped Vpg/Ver, bit by bit inhibit, prog. ref. cells
- MLC

Close-Loop Intelligent Hardware Controller:

- Manage HDD files
- Host Independent, Standard mass storage I/O
- Dynamically manage defective bits/sectors (ECC, retry, recovery, substitution, links)
- Wear-out leveling, hot count
- Adaptive W/E voltages

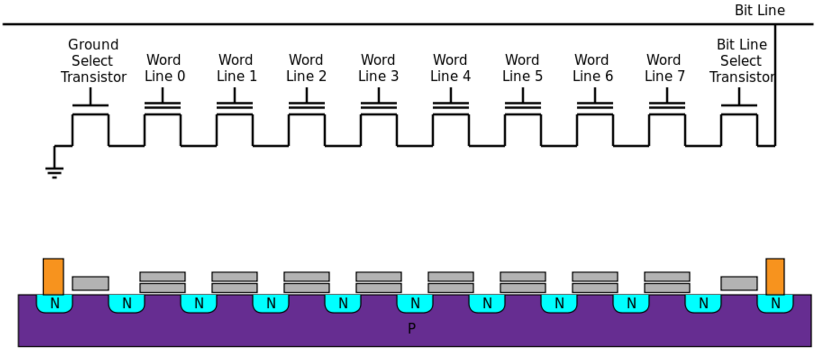
NOR Flash

- Random, direct access interface.
- Fast random reads.
- Slow erase/writes.

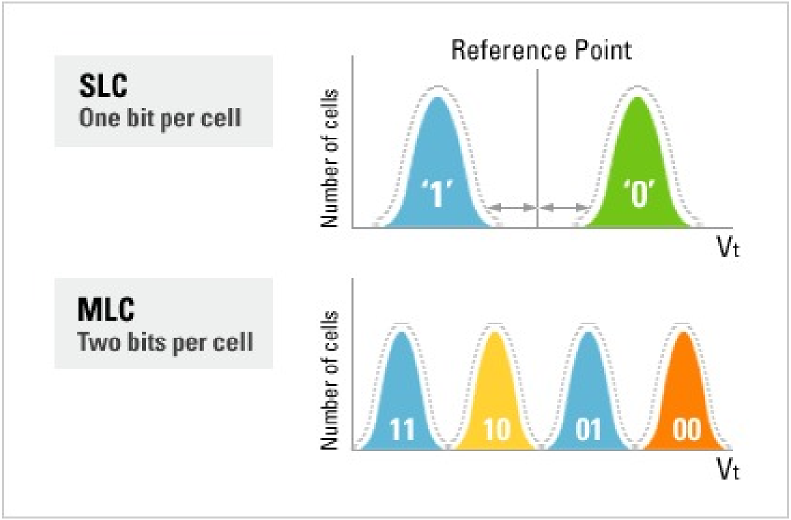


NAND Flash

- Higher density, lower cost.
- Fast erase/write.
- Block input/output access.

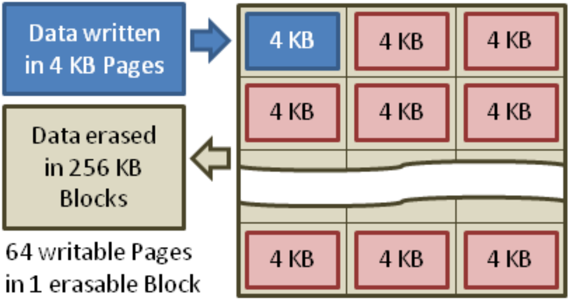


Single, Multi, and 3-bit Level Flash Cells



Block Level Access

- Minimal working unit, depends on size/technology.
- No read/write operation simultaneously.
- Erasing a block sets all bits to 1.
- Programming changes bits from 1 to 0.

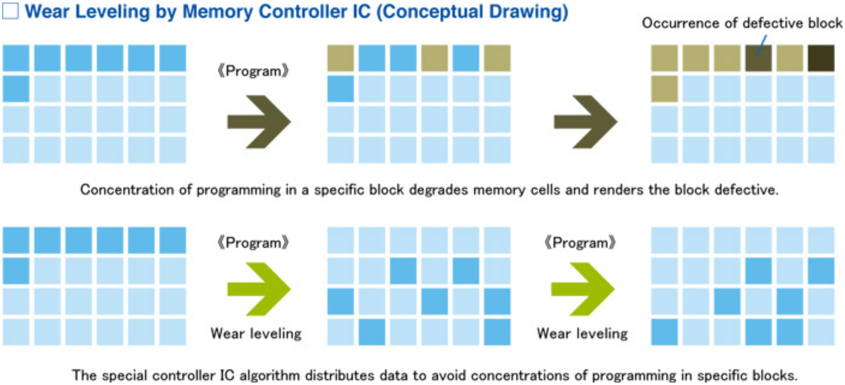


Typical NAND Flash Pages and Blocks

Data Retention

Finite number of P/E cycles.

- Wear leveling.
- Bad block management.



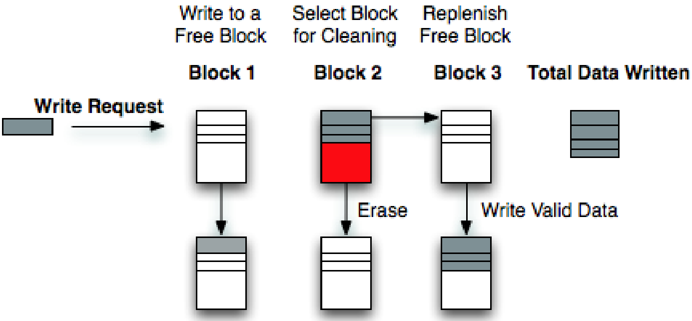
☐ **Wear Leveling by Memory Controller IC (Conceptual Drawing)**

Concentration of programming in a specific block degrades memory cells and renders the block defective.

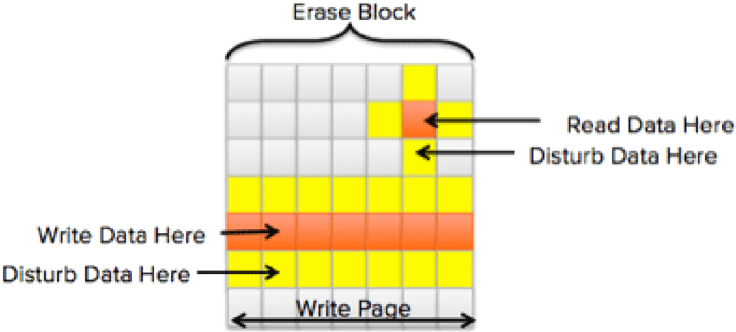
The special controller IC algorithm distributes data to avoid concentrations of programming in specific blocks.

Write Amplification

$$\text{write amplification factor} = \frac{\text{data that controller has to write}}{\text{data that host wants to write}}$$



Write and Read Disturb



Summary

- block-level access
- wear leveling
- read disturb
- bad blocks management
- garbage collection
- different physics
- different interfaces

Sources

- http://persianwondersvideo.blogspot.co.il/2007/02/jiroft.html
- http://en.wikipedia.org/wiki/Eprom
- http://en.wikipedia.org/wiki/Flash_memory
- http://www.monolithic3d.com/2/post/2011/11/what-can-we-learn-from-the-success-of-eli-harari-and-s
  html